Opportunities and challenges of silicon photonics based System-In-Package

ECTC 2014

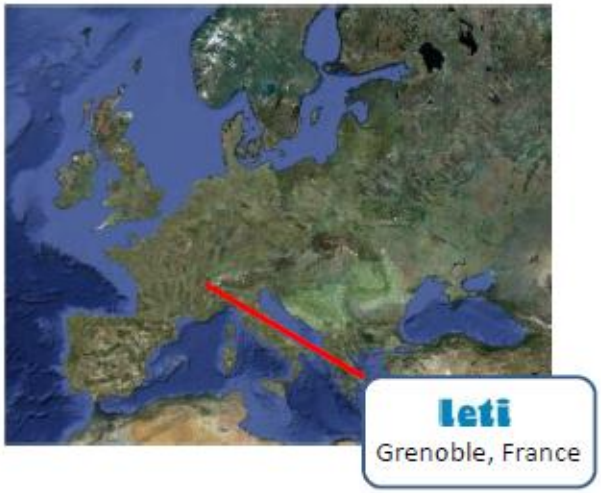
Panel session : *Emerging Technologies and Market Trends of Silicon Photonics*

Speaker : Stéphane Bernabé (Leti – Photonics Department)

Presentation built with help from colleagues at the Silicon Photonics lab (S. Menezo, L. Fulbert) , and at the 3D Packaging team (Y. Lamy, H. Ben Jamaa, P. Leduc, G. Pares)

Silicon Photonics at Leti

French R&D institute in microelectronics & nanotechnologies from



1,700 researchers

Over 2,200 patents

250 M€ annual budget

50 start-ups
& 365 industrial partners

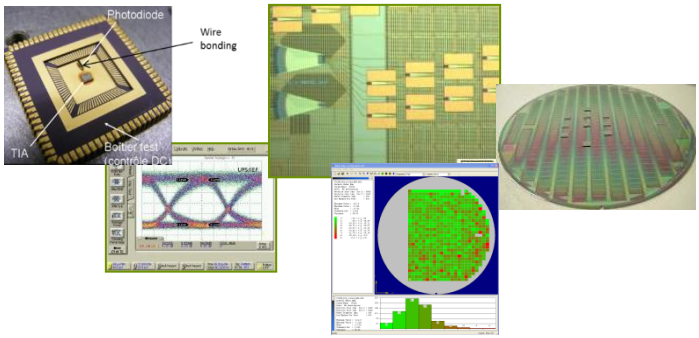
- ~100 people working on 3D IC and 3D Packaging
- Full 200mm & 300mm 3D capabilities

Silicon Photonics

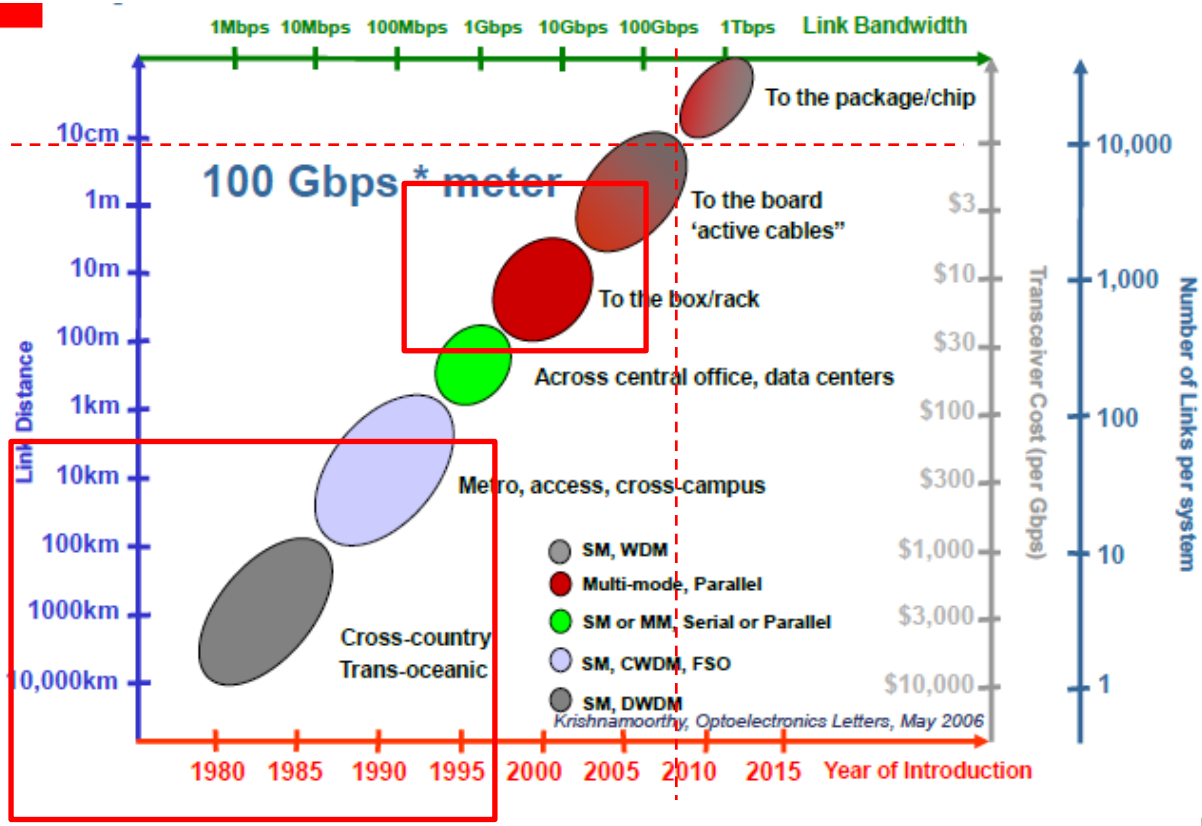
A dedicated lab involved in :

- **Component and circuits design**
- **Modeling**
- **Module integration**
- **On-wafer characterization**

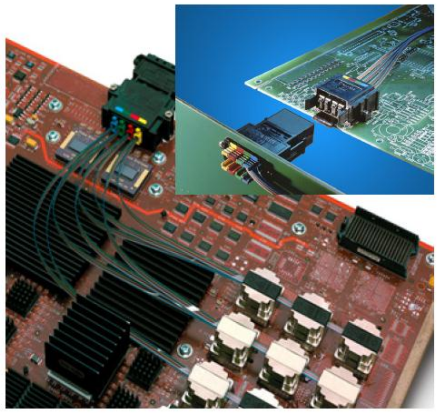
200 mm and 300mm PIC *(Photonic Integrated Circuits)* manufacturing on SOI wafers



Silicon Photonics : roadmap

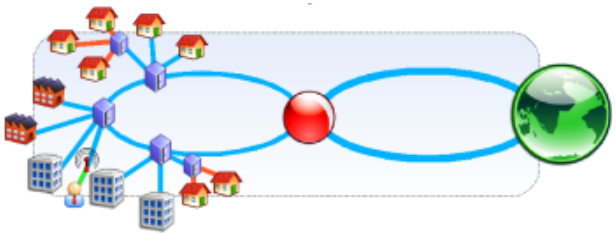


Source : Brocade



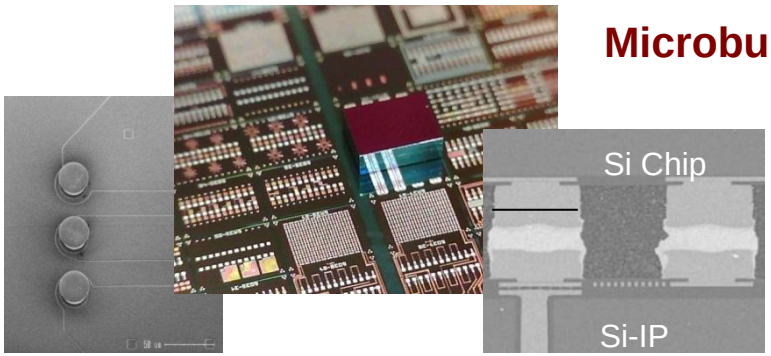
On-board modules

Data centers : AOC

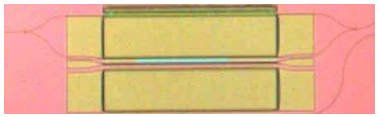


Telecom Networks

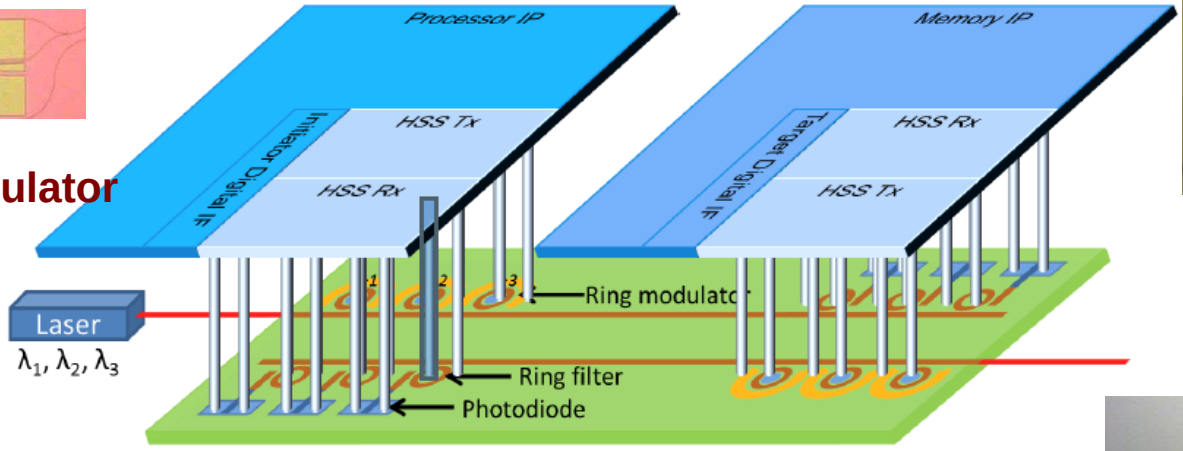
Building blocks

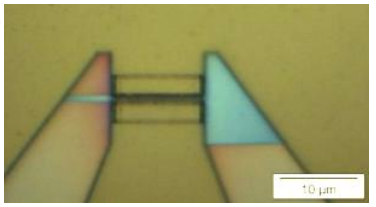


Microbumps

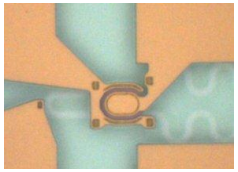


Optical modulator
up to 40Gb/s

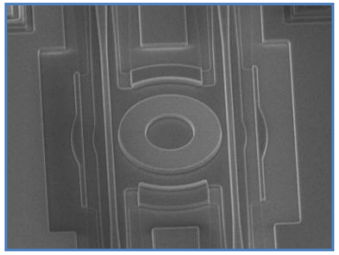




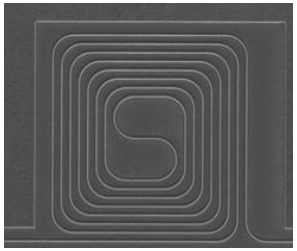
Photodetector
up to 40Gb/s



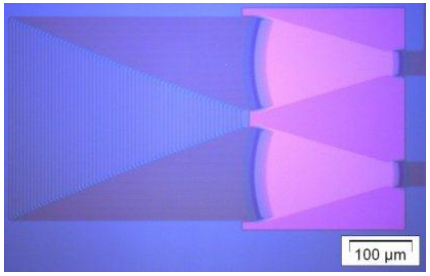
Laser source



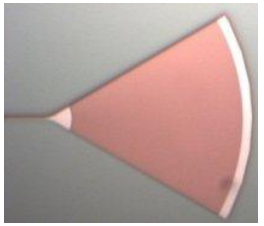
Ring modulator



Waveguides



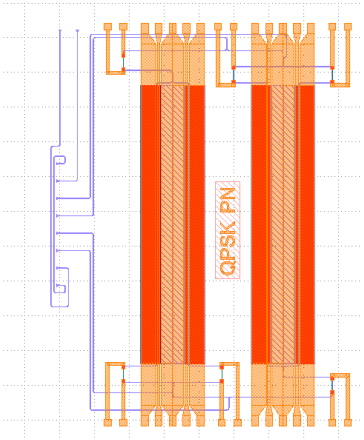
WDM filters

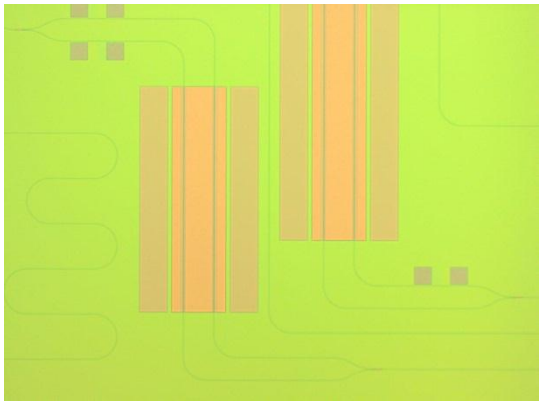


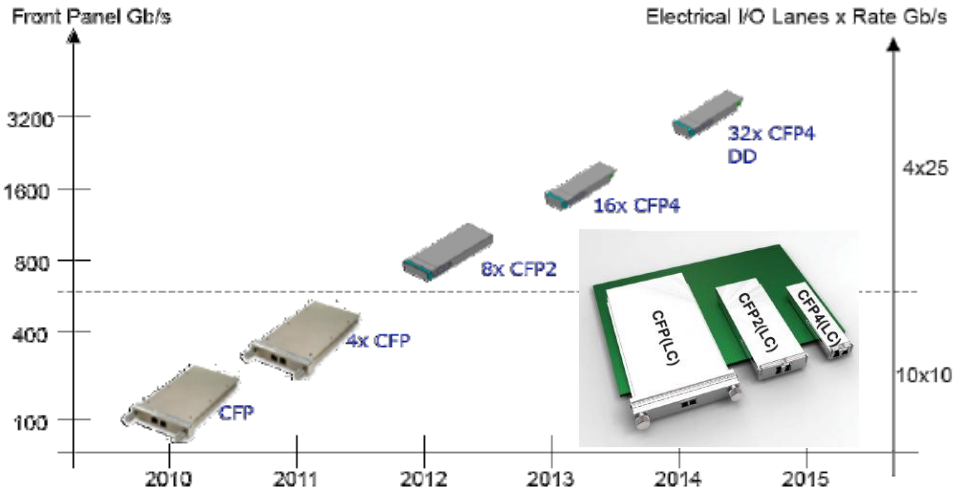
Fiber coupler

Opportunities for Silicon Photonics PICs

- Key enabler for high complexity PICs
  - Modulation / photodetection / WDM filtering on the same chip
  - Integrated laser for Tx or local oscillator
  - Enabler for PDM-QPSK modulation format
- Very High Density Interconnections & aggregated bandwidth, w/ WDM
  - Enabler for Tbps applications
- Scalable architectures
- Mass production volume
  - CMOS compatible
- Today , pushed by 100G module standards
  - Decreasing form factors
  - CFP modules
  - Cisco's CPAK module

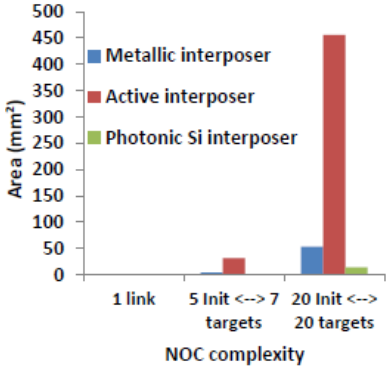


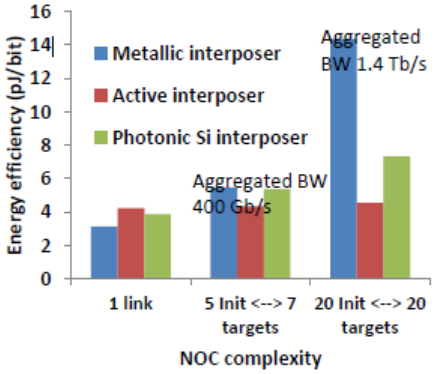


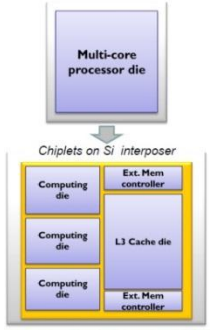


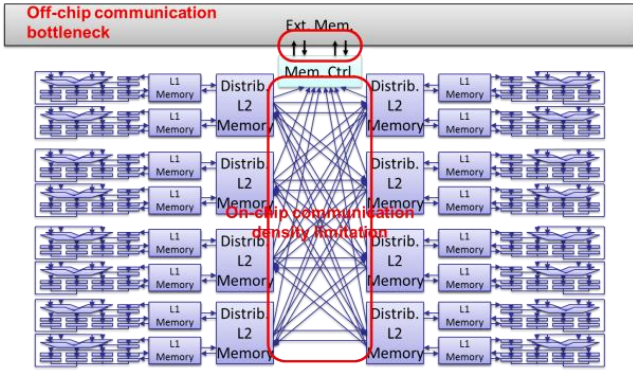
Optical Network on chip

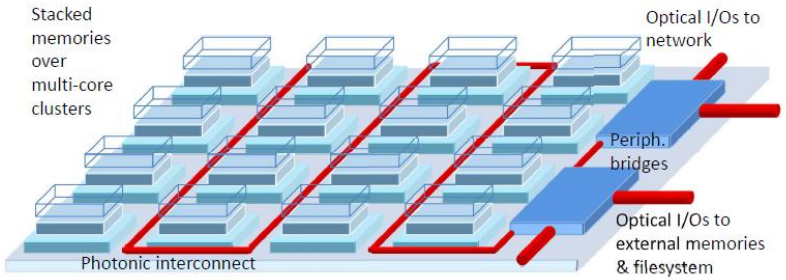
- Address manycore architectures
- Low latency, multiple access
- Make use of SOI photonics chips as interposer (System On Package)







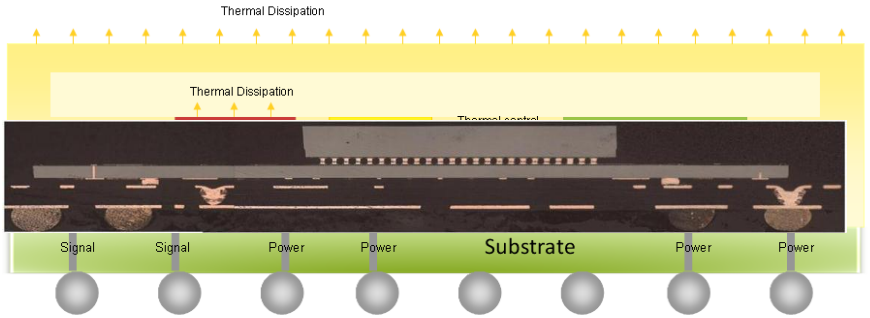




➔Integration of multiple advanced technologies

➔External IP, interface standards, supply chain

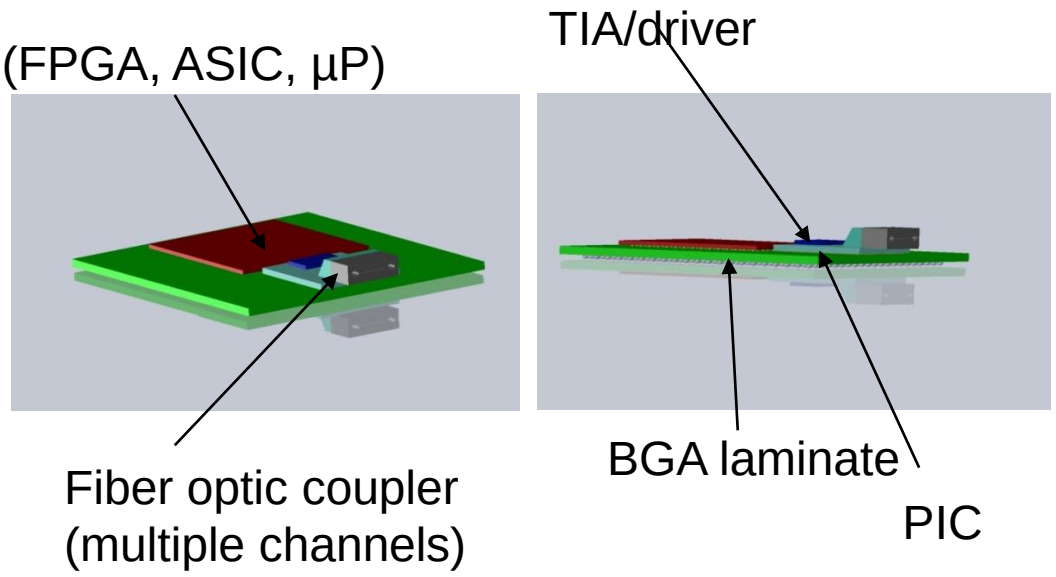
➔Metallic interposer optimal for less than 4 init/targets
➔Active interposer is best for intermediate number of cores (5~10 init/targets)
➔Photonics becomes relevant for many-core system (>20)
➔Photonic link yet requires improvement on energy efficiency performances: from 10 pJ/bit to 100 fJ/bit in 2020

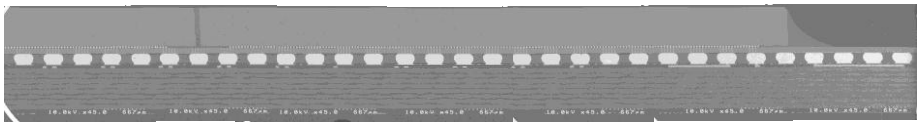


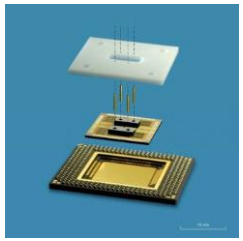
From Y. Thonnart, Optical Systems on Chip: a Physical Perspective, FETCH Winter School, January 10th, 2014|

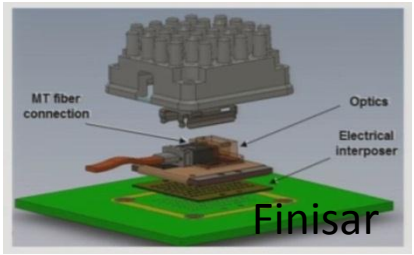
Silicon photonics based SiP

- Rationale
  - 2D use of the board
  - Provide optical IOs to large EICs
- Targeted applications
  - Intra-rack
  - Intra-board
  - HPC
- VCSEL modules have already switched to SiP architectures
  - BGA style packages
  - No standard at the moment

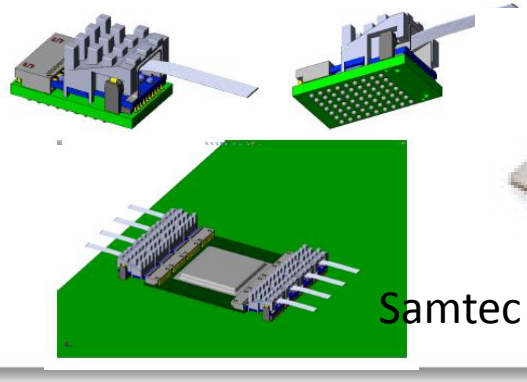








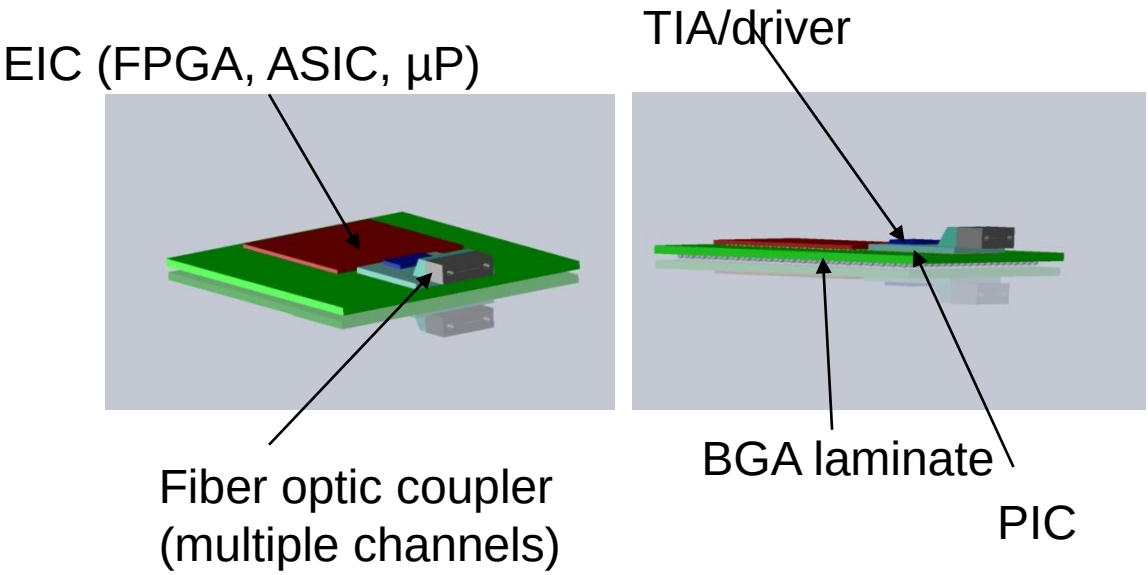
Finisar

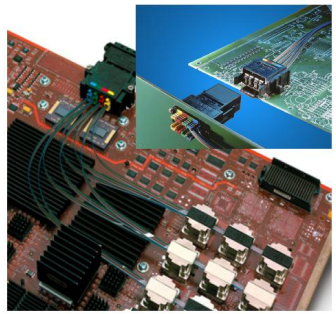

Samtec

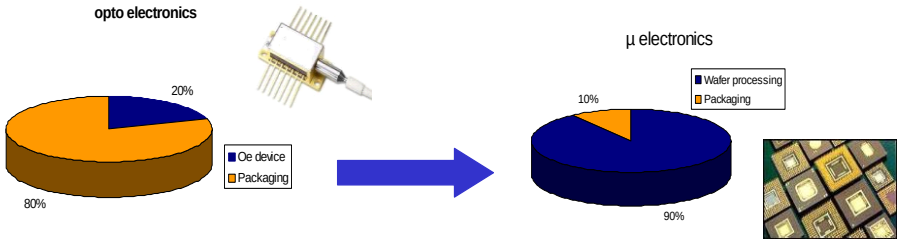
Avago/Altera

Requirements

- High channel density
  - Multichannel compatible (mix WDM+Parallel)
- Low footprint
  - But high I/O count
- Low profile
  - Blade server compatible
- High Bandwidth/data rate
  - up to 25Gbps
- Multifiber Optical plug/connector
- CMOS process compatible
  - And SMD process compatible
- High throughput… and low cost



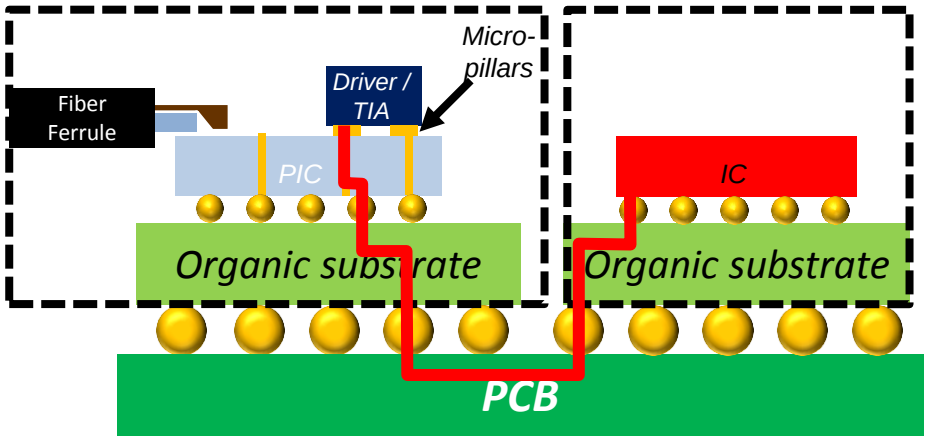




Packaging scenarios

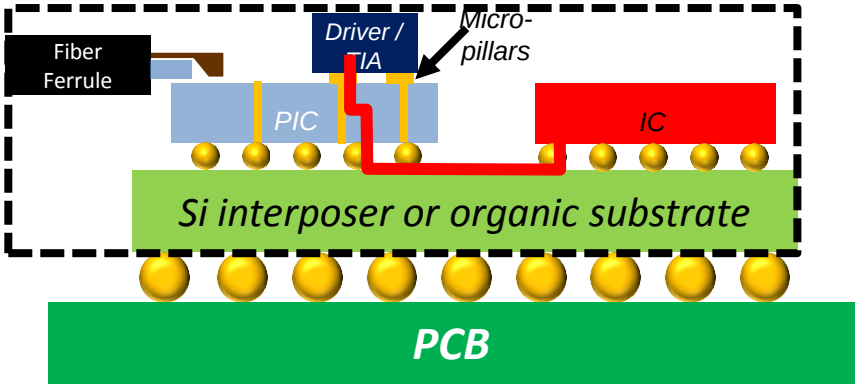
Standalone module

Electrical path trough Levels 0, 1, 2 + PCB→
BW and power consumption limitations
Flexible



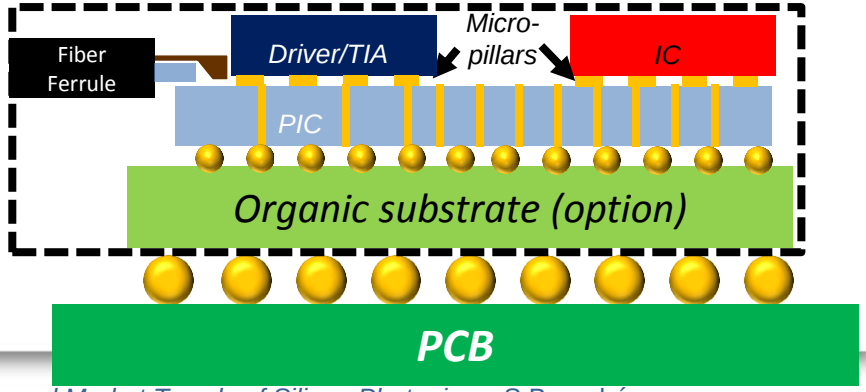
Co-packaging with optical transceiver

Electrical path trough Levels 0, 1, 2
Co-packaging challenging: thermal issues, supply chain
Partitionning to be evaluated



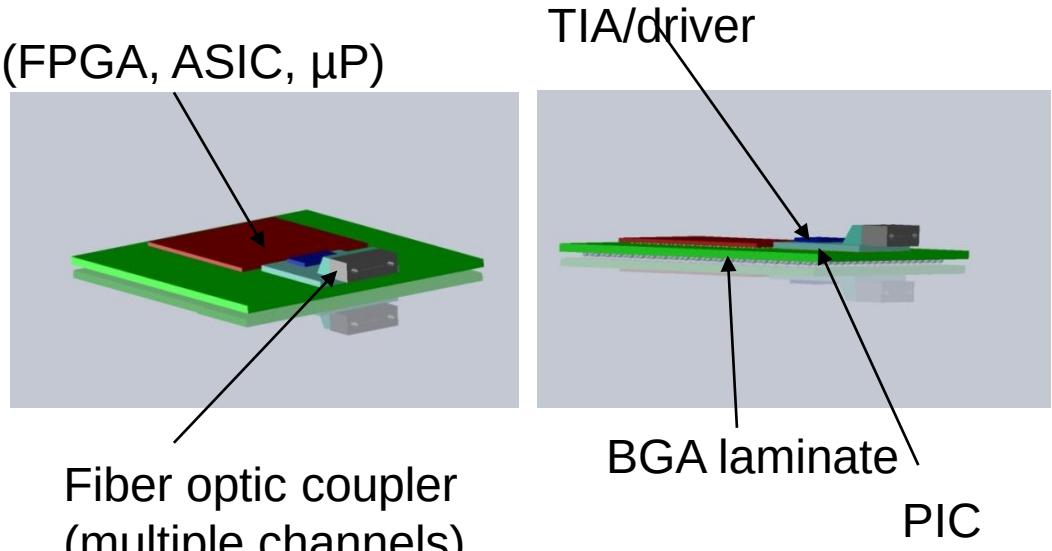
Photonic interposer

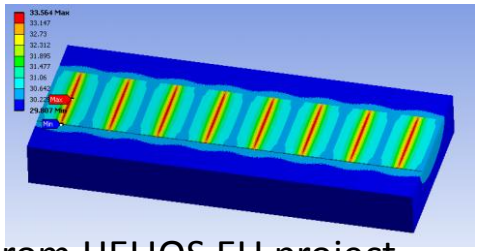
Electrical path trough Levels 0, 1
Co-packaging challenging: thermal issues, supply chain, cost of large photonic interposer



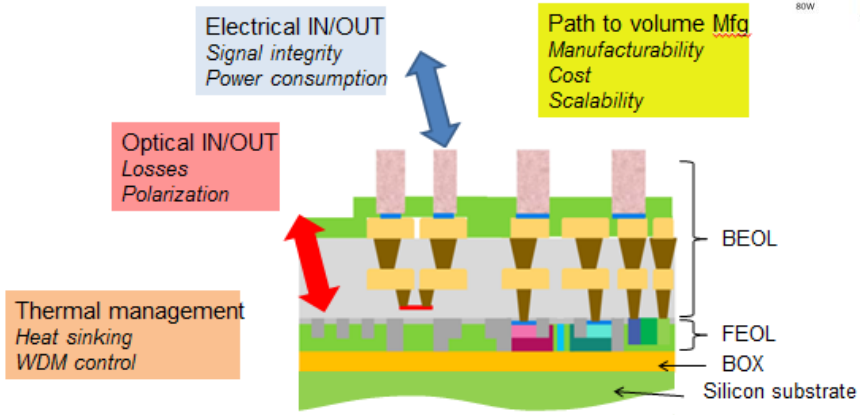
Challenges

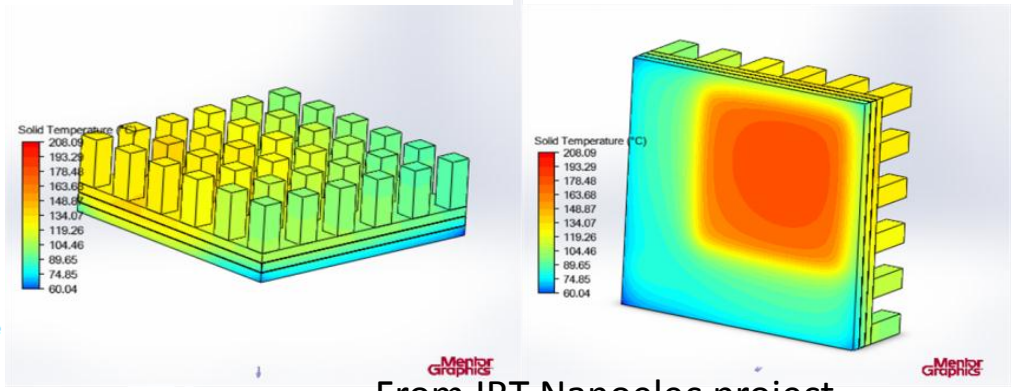
- Laser integration
- RF management
- Optical coupling
- Thermal management
  - Could be a killer
  - T sensitive functions
  - Hot spots





From HELIOS EU project

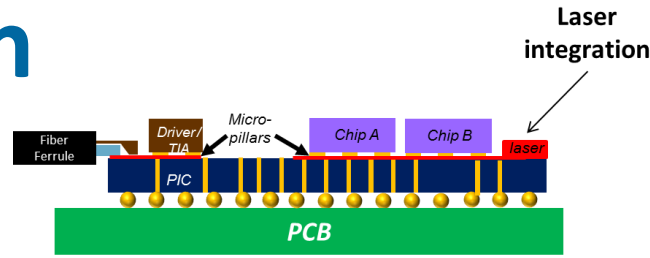


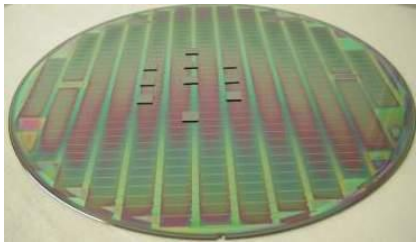


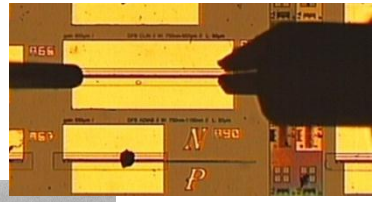
From IRT Nanoelec project

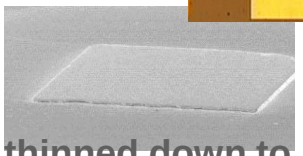
Challenge : laser integration

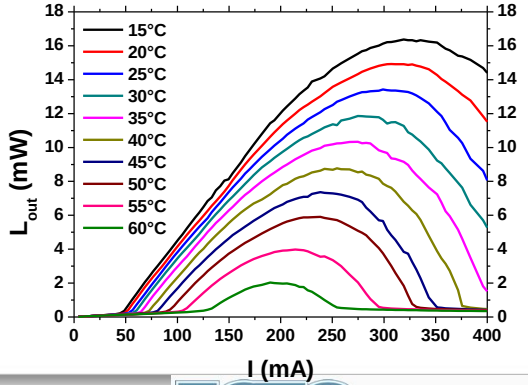
- Alignment of laser structure / waveguides
- CW operation @ λ = 1.57µm , SMSR~20dB
- Key Enabling technology for integrated multi-lambda sources, up to 10mW coupled power

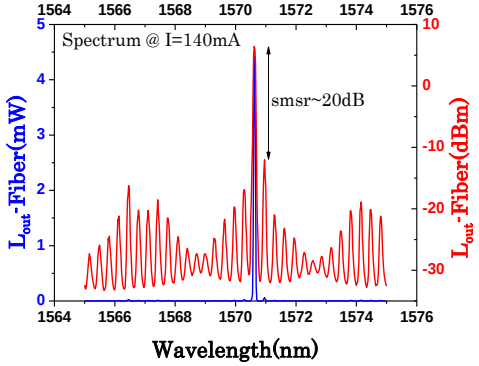


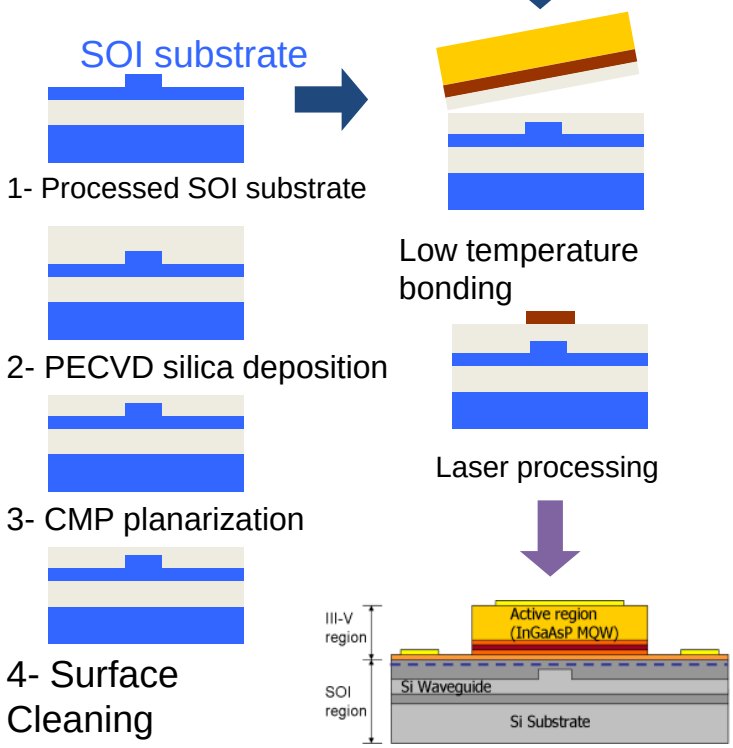






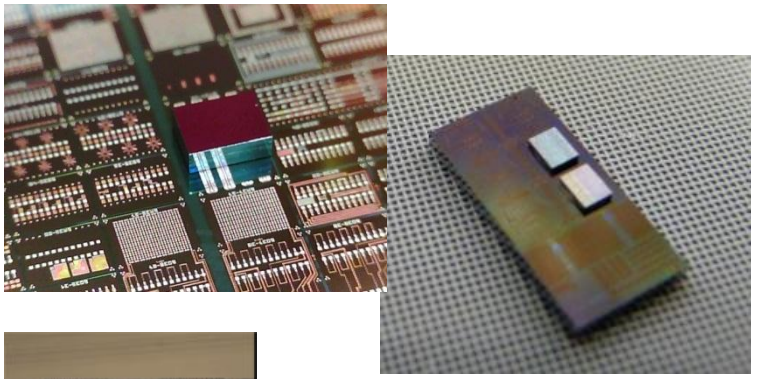


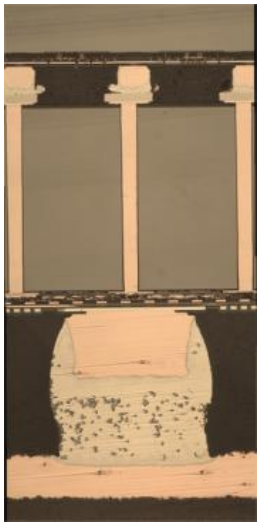


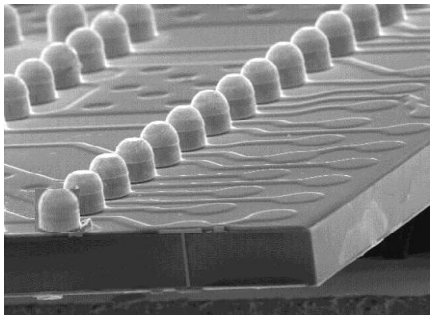


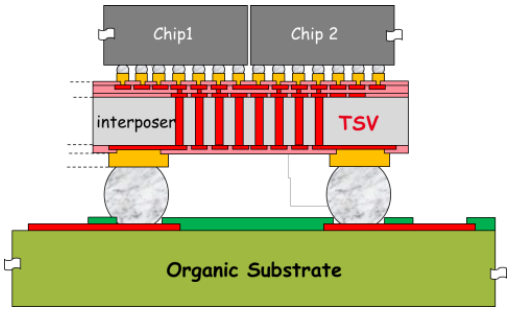
Challenges : RF & 3D

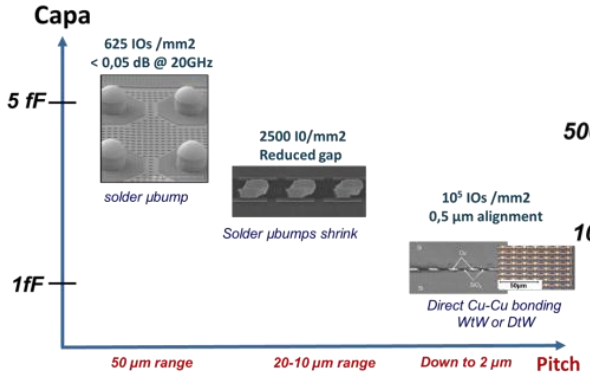
- 3D packaging is a key technologies for future Silicon Photonics devices
- Rationale for hybrid integration
  - KGD approach, Standard assembly technology, high yield
  - Short RF lines between photonics functions and related ASICs (TIA, Drivers)
  - Chip size independant
- Flip-chip assembly advantages
  - Copper/SAC microbumps
  - Low inductance compared to wire-bonding
  - High density (pitch 40µm, or lower)
  - Low capacitance (<10 fF)

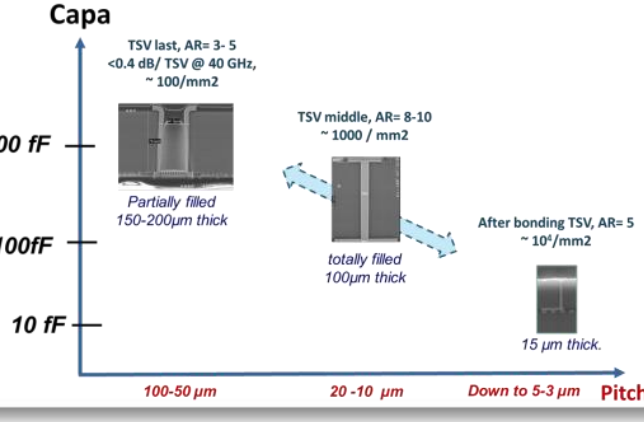






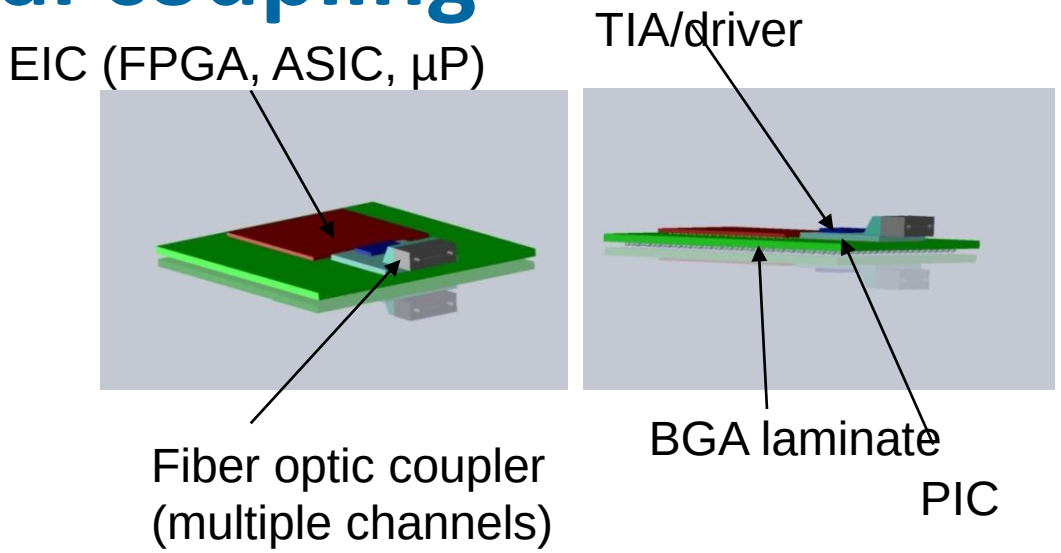






Challenges : optical coupling

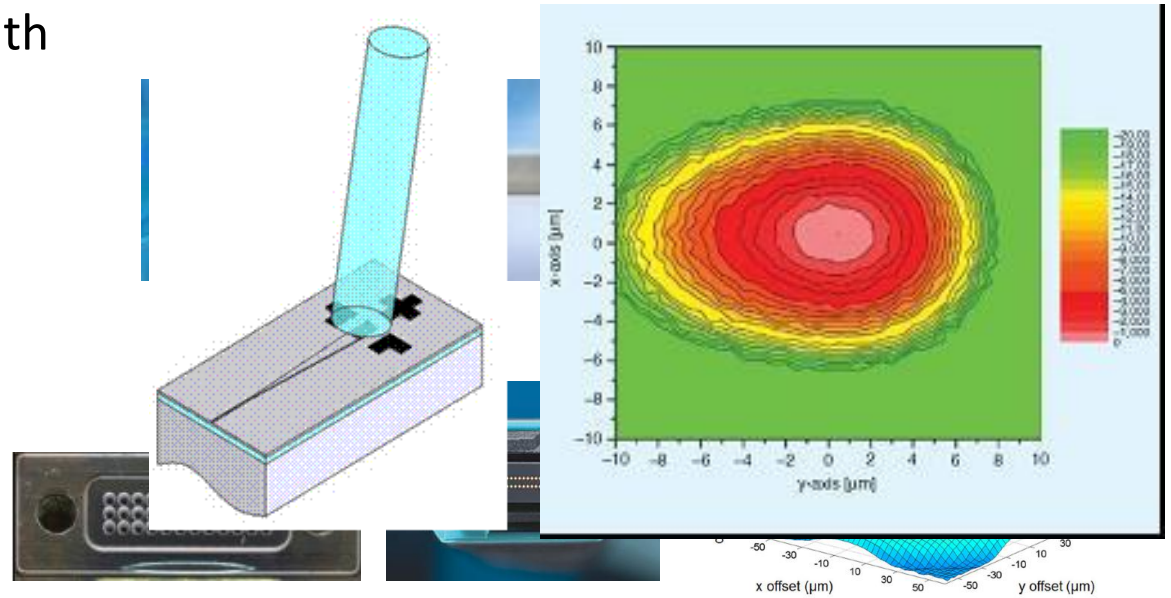
- Use of vertical grating couplers
  - On wafer test capability, 2D IO enabling
  - Matched MFD for SMF butt coupling
    - Moderate coupling losses



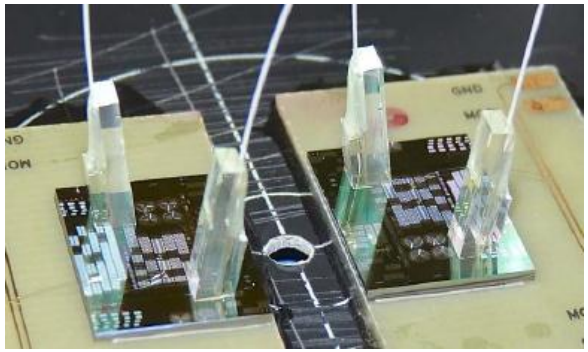
- Vgroove array combined with active alignment

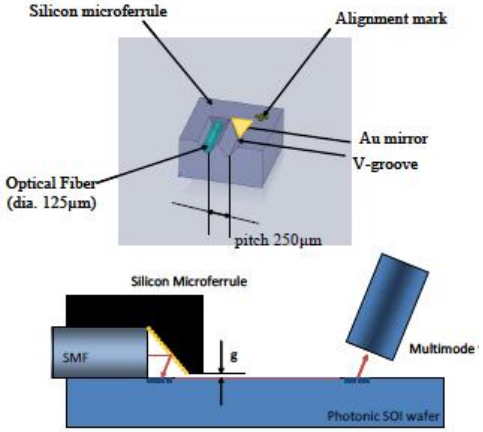
- 2D and Lensed MT-based connectors

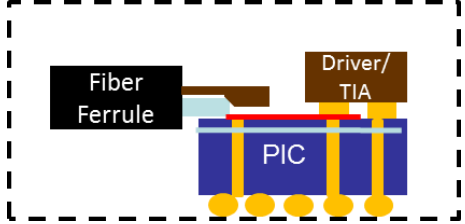
- Multicore fiber
  - Typ. 40µm pitch, 7 cores/fiber

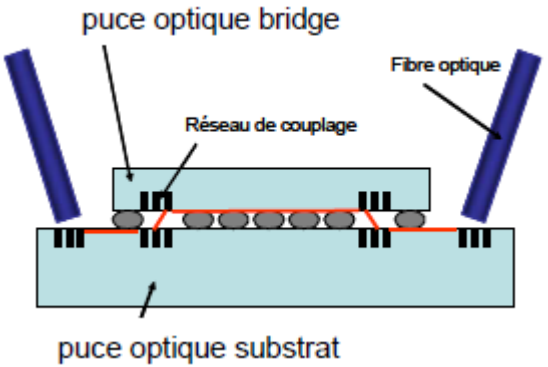


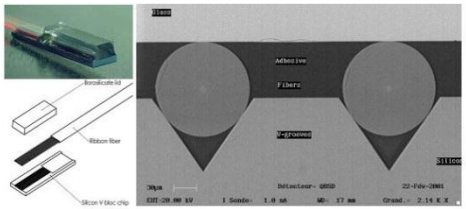
Optical coupling toolbox

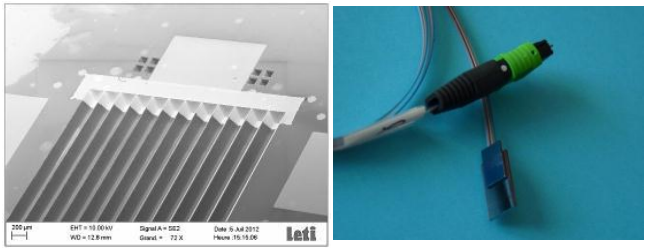


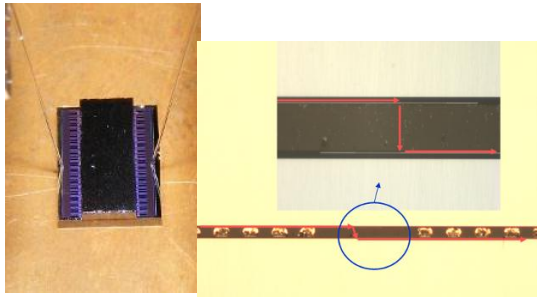












Active alignement	Semi-passive alignement	Passive alignement
Typical penalty 0.2 dB single fiber 0.5-1dB dB fiber array Assembly time: <5 min Unitary process (pigatiling)	Vision assisted alignement Silicon etched groove ferrules 2.5 to 4 dB penalty loss Assy time ~1 min High throughput assembly of the fiber holder (Pick & place)	Vertical Grating coupler Self alignement In solder bumps Excess loss due to misalignement < 1dB Fully collective process (reflow)

Conclusion

- Silicon Photonics is a key enabler for Terabit VSR optical links
- The natural trend for this class of application is to use microlectronic-like modules, especially through System-In-Package approach
- For this kind of module, several specific challenges have to be adressed
  - Thermal
  - RF links & related power consumption
  - Optical coupling
- For most of these challenges, 3D packaging toolbox provides solutions
- Photonic Integrated Circuits and 3D packaging need to be merged in order to build very high density optical modules

Leti

LABORATOIRE D'ÉLECTRONIQUE
ET DE TECHNOLOGIES
DE L'INFORMATION

CEA-Leti
MINATEC Campus, 17 rue des Martyrs
38054 GRENOBLE Cedex 9
Tel. +33 4 38 78 36 25

www.leti.fr